AMENDMENTS TO THE CLAIMS

Please cancel claims 37-113. The remaining claims are provided below.

1. (Original) An n-bit digital potentiometer including 2^n wiper positions, comprising:

a first reference terminal, an opposite second reference terminal, and a wiper terminal;

a string of approximately same impedance elemental impedance devices, said string having first and second end terminals;

a plurality of wiper switches each coupled between the wiper terminal and the first string; and

a bulk impedance device having a first end coupled to the first end terminal of the first string, an opposite second end, and an impedance value greater than an impedance of the string of elemental impedance devices,

wherein the string and the bulk impedance device are between the first and second reference terminals, and the second end terminal of the first string and the second end of the bulk impedance device are each switchable between a coupling to the first reference terminal and a coupling to the second reference terminal.

2. (Original) The digital potentiometer of claim 1, further comprising first and second switching devices operable to implement the switchable coupling of the first end terminal of the first string to the first and second reference terminals, and the switchable coupling of the second end of the bulk impedance device to the first and the second reference terminal, in a complementary manner,

wherein the first switching device is coupled between the first end terminal of the first string, the first reference terminal, and the second reference terminal, and the second switching device is coupled between the second end of the bulk impedance device, the first reference terminal, and the second reference terminal.

3. (Original) The digital potentiometer of claim 2, wherein first switching device includes a first transistor coupled between the first end terminal of the first string and the first reference terminal, and a second transistor coupled between the first end terminal of the first string and the second reference terminal, and

wherein the second switching device includes a first transistor coupled between the second end of the bulk impedance device and the second reference terminal, and a second transistor coupled between the second end of the bulk impedance device and the first reference terminal.

4. (Original) The digital potentiometer of claim 2, wherein the first and second switching devices are controlled based on a most significant bit of an input n-bit wiper address.

5. (Original) The digital potentiometer of claim 1, wherein the switchable coupling of the first end terminal of the first string and the second end of the bulk impedance device are controlled in a complementary manner based on a most significant bit of an input n-bit wiper address.

6. (Original) The digital potentiometer of claim 5, wherein a switching of the wiper switches is controlled based on bits of

the input n-bit wiper address other than the most significant bit of the wiper address.

7. (Original) The digital potentiometer of claim 1, wherein the impedance of the bulk impedance device is approximately 2^{n-1} times the impedance of one of the elemental impedance devices.

8. (Original) The digital potentiometer of claim 7 wherein the digital potentiometer has $2^{n-1}-1$ said elemental impedance devices, and 2^{n-1} said wiper switches.

9. (Original) The digital potentiometer of claim 1, wherein the impedance of the first string is less than the impedance of the bulk impedance device by an amount approximately equal to the impedance of one of the elemental impedance devices.

10. (Original) The digital potentiometer of claim 1 wherein the digital potentiometer has $2^{n-1}-1$ said elemental impedance devices, 2^{n-1} said wiper switches, the impedance of the bulk impedance device is approximately 2^{n-1} times the impedance of one of the elemental impedance devices, and the complementary switching of the first end terminal of the first string and the second end of the bulk impedance device is controlled based on a most significant bit of an input n-bit wiper address.

11. (Original) An n-bit digital potentiometer including 2^n wiper positions, comprising:

a first reference terminal, an opposite second reference terminal, and a wiper terminal;

a string of $2^{n-1}-1$ approximately same impedance elemental impedance devices, wherein a first end of the string is coupled to the wiper terminal;

a plurality of wiper switches each coupled between the wiper terminal and the string; and

at least one bulk impedance device, wherein the at least one bulk impedance device has an impedance approximately 2^{n-1} times the impedance of one of the elemental impedance devices, and the string and the at least one bulk impedance device are disposed between the first and second reference terminals.

12. (Original) The digital potentiometer of claim 11, further comprising at least one switching device, wherein operation of the at least one switching device causes the string to alternate between providing wiper positions in a lower half of the 2^n wiper positions and in an upper half of the 2^n wiper positions.

13. (Original) The digital potentiometer of claim 12, wherein the at least one bulk impedance device is a single bulk impedance device, and the single bulk impedance device is coupled to the first end of the string.

14. (Original) The digital potentiometer of claim 12 wherein the string has a second end opposite the first end, the at least one switching device is two switching devices, with one of the two switching devices coupled between the second end of the string and the first reference terminal, and the other of the two switching devices coupled between the single bulk impedance device and the second reference terminal.

15. (Original) The digital potentiometer of claim 12, wherein the string alternates between providing wiper positions in a lower half of the 2^n wiper positions and in an upper half of

the 2^n wiper positions during operation of the digital potentiometer.

16. (Original) The digital potentiometer of claim 11, wherein the at least one bulk impedance device is first and second bulk impedance devices, the at least one switching device is first and second switching devices, and the string includes a second end opposite the first end, and

wherein the first bulk impedance device and the first switching device are coupled to the first end of the string and the first reference terminal, with the first switching device being operable to bypass the first bulk impedance device, and the second bulk impedance device and the second switching device are coupled to the second end of the string and the second reference terminal, with the second switching device being operable to bypass the second bulk impedance device.

17. (Original) The digital potentiometer of claim 16, wherein the first and second switching devices are operable in a complementary manner based on a most significant bit of an input n-bit wiper address.

18. (Original) The digital potentiometer of claim 12, wherein the at least one bulk impedance device is first and second bulk impedance devices, the at least one switching device is first and second switching devices, the first switching device is operable to bypass the first bulk impedance device, and the second switching device is operable to bypass the second bulk impedance device.

19. (Original) The digital potentiometer of claim 18, wherein the first and second switching devices are operable in a

complementary manner based on a most significant bit of an input n-bit wiper address.

20. (Original) An n-bit digital potentiometer including 2^n wiper positions, comprising:

a first reference terminal, an opposite second reference terminal, and a wiper terminal;

a string of approximately same impedance elemental impedance devices;

at least one bulk impedance device, wherein the string and the at least one bulk impedance device are disposed between the first and second reference terminals, and the at least one bulk impedance device has an impedance greater than an impedance of the string;

a plurality of wiper switches each coupled between the wiper terminal and the string; and

a control circuit that receives an input n-bit wiper address, and based thereon controls both a switching of the wiper switches and a selection between having the string provide wiper positions in a lower half of the 2^n wiper positions and in an upper half of the 2^n wiper positions.

21. (Original) The digital potentiometer of claim 20, wherein the control circuit selects between having the string provide

wiper positions in the lower half of the 2^n wiper positions and in the upper half of the 2^n wiper positions based on a first subportion of the input n-bit wiper address, and controls the switching of the wiper switches based on a different second subportion of the n-bit wiper address.

22. (Original) The digital potentiometer of claim 20, wherein the at least one bulk impedance device is a single bulk impedance device.

23. (Original) The digital potentiometer of claim 19, wherein the at least one bulk impedance device is a first bulk impedance device and a second bulk impedance device, with the first bulk impedance device being coupled between a first end of the string and the first reference terminal, and the second bulk impedance device being coupled between an opposite second end of the string and the second reference terminal, and

wherein the control circuit controls a selective bypassing of the first bulk impedance device, and a selective bypassing of the second bulk impedance device.

24. (Original) A method of operating an n-bit digital potentiometer having 2^n impedance units between a first reference terminal and a second reference terminal, the method comprising:

disposing an n-bit wiper address in the digital potentiometer, said digital potentiometer including a first string of elemental impedance and a bulk impedance device between the first and second reference terminals, the bulk impedance device having an impedance greater than an impedance of the first string, wherein a first end of the string is coupled to a first end of the bulk impedance device;

alternating a coupling of the second end of the first string and the second end of the bulk impedance device to the first reference terminal and to the second reference terminal based on the first n-bit wiper address; and

tapping the first string based on the first n-bit wiper address.

25. (Original) The method of claim 24, wherein the step of alternating the coupling is based on only a most significant bit of the n-bit wiper address.

26. (Original) The method of claim 24, wherein the digital potentiometer has 2^{n-1}-1 said elemental impedance devices, and an impedance of the bulk impedance device is approximately 2^{n-1} times the impedance of one of the elemental impedance devices.

27. (Original) A method of operating an n-bit digital potentiometer having 2^n wiper positions, a first reference terminal and a second reference terminal, the method comprising:

disposing an n-bit wiper address in the digital potentiometer, said digital potentiometer including a first string of 2^{n-1}-1 approximately same impedance elemental impedance devices and at least one bulk impedance between the first and second reference terminals, the at least one bulk impedance device having an impedance approximately 2^{n-1} times the impedance of one of the elemental impedance devices;

alternating the first string between providing impedance in a lower half of the 2^n wiper positions and an upper half of the 2^n wiper positions based on a first subportion of the n-bit wiper address, with the at least one bulk impedance device providing impedance in the one of the lower half and the upper half of the 2^n wiper positions not provided by the first string; and

tapping the first string based on a second subportion of the n-bit wiper address.

28. (Original) The method of claim 27, wherein the at least one bulk impedance device is a single bulk impedance device, and the step of alternating the first string comprises:

coupling the first string to the first reference terminal to have the first string provide impedance in the lower half of the 2^n wiper positions and to the second reference terminal to provide impedance in the upper half of the 2^n wiper positions, and coupling the single bulk impedance device to the one of the first and second reference terminals not coupled to the first string.

29. (Original) The method of claim 28, wherein a first structure also is between the first and second reference terminals, said first structure comprising an impedance device and a permanently-on switch.

30. (Original) The method of claim 27, wherein the at least one bulk impedance device comprises two bulk impedance devices, with one of the bulk impedance devices being coupled between the first reference terminal and a first end of the first string and the other of the bulk impedance devices being coupled between the second reference terminal and a second end of the first string, and

wherein the step of alternating the first string comprises bypassing one of the bulk impedance devices and not bypassing the other of the bulk impedance devices.

31. (Original) The method of claim 30, wherein a first structure also is between the first and second reference terminals, said first structure comprising an impedance device and a permanently-on switch.

32. (Original) The method of claim 27, wherein a first structure also is between the first and second reference

terminals, said first structure comprising an impedance device and a permanently-on switch.

33. (Original) An n-bit digital potentiometer including 2^n wiper positions, comprising:

a first reference terminal, an opposite second reference terminal, and an wiper terminal;

a first string of approximately same impedance elemental impedance devices, said first string having opposed first and second end terminals;

a plurality of wiper switches each coupled between the wiper terminal and the first string; and

at least one bulk impedance device having an impedance greater than an impedance of the first string,

wherein the first string and the at least one bulk impedance device are disposed between the first and second reference terminals, and

wherein the at least one bulk impedance device is coupled between the first reference terminal and the first string when an input n-bit wiper address has a logical one most significant bit and is coupled between the second reference terminal and the first string when the most significant bit of the input n-bit wiper address is a logical zero.

34. (Original) The digital potentiometer of claim 33, wherein the at least one bulk impedance device is a single bulk impedance device selectively coupleable to the first and second reference terminals.

35. (Original) The digital potentiometer of claim 33, wherein the at least one bulk impedance device comprises first and second bulk impedance devices, with the first bulk impedance

device being coupled between the first reference terminal and the first end terminal of the first string, and the second bulk impedance device being coupled between the second reference terminal and the second end terminal of the first string, and

wherein a first switching device is coupled to the first reference terminal, and second switching device is coupled to the second reference terminal, the first switching device being operable to bypass the first bulk impedance device, and the second switching device being operable to bypass the second bulk impedance device.

36. (Original) The digital potentiometer of claim 33, further comprising mirror image second and third strings of shunted impedance devices also between the first and second reference terminals, wherein an impedance of each of the second and third strings is between the impedance of the first string and the impedance of the at least one bulk resistor.

37-113. (Cancelled)